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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/597,190	06/20/2000	William P. Bunton	1662-29000 (P00-3000)	5908

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EXAMINER	
DUONG, FRANK	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/597,190	BUNTON ET AL.	
	Examiner	Art Unit	
	Frank Duong	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,11 and 14-18* is/are rejected.

7)☒ Claim(s) *9,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/00*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to the communication dated 06/20/2000. Claims 1-18 are pending in the application.

Information Disclosure Statement

2. The information disclosure statement filed 11/13/2000 complies with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609. It has been considered and placed in the application file.

Claim Objections

3. Claim 9 is objected to because of the following informalities: Lines 2 and 3, "the first word" and "the second word" should read --a first word-- and --a second word--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-8, 10-11 and 14-18 are rejected under 35 U.S.C. 102(e) as being

anticipated by Drotter et al (USP 6,646,991) (hereinafter "Drotter").

Regarding **claim 1**, in accordance with Drotter reference entirety, Drotter discloses a high speed interconnection link (Fig. 4) that comprises:

a receiver (113) configured to receive a plurality of channels(108-111) (*col. 3, lines 46-54*);

a receiver logic circuit (118-121) configured to receive signals from each of the plurality of channels (108-111) and monitor the signals for symbols (A1-A4) that are unique to each channel, wherein upon detecting unexpected symbols (*col. 4, line 28; unexpected cell*) in the channels (links), the receiver logic circuit is configured to correct the order of the channels (*col. 3, lines 55-60 and col. 4, lines 20-55 and col. 5, lines 3-20 reading in reference to Fig. 9*).

Regarding **claim 2**, in addition to features recited in base claim 1 (see rationales discussed above), Drotter further discloses a transmitter (100) coupled to the plurality of channels (108-111) and a transmitter logic circuit (101-103) configured to transmit signals to corresponding channels, wherein the transmitter logic circuit is configured to reorder the correspondence of the signals transmitted to the channels (*col. 3, lines 46-54 and col. 5, lines 23-43*).

Regarding **claim 3**, in addition to features recited in base claim 2 (see rationales discussed above), Drotter further discloses wherein the transmitter logic circuit (101-103) comprises a bank of multiplexers (103 and 104-107) each configured to transmit a selected one of two input signals to be transmitted through a channel (any of 108-111) (*note: disclosed round robin controller is equated to corresponding to "a bank of*

multiplexers" because of its selection of signal for transmitting in combination with interfaces 104-107 and logic 101-102).

Regarding **claim 4**, in addition to features recited in base claim 1 (see rationales discussed above), Drotter further discloses wherein the receiver logic circuit (118-121) comprises a bank of multiplexers (118) each configured to transmit a selected one of two input signals (signal received at 114-117) received from a channel (any of 108-111) (*note: disclosed incoming message buffers is equated to corresponding to "a bank of multiplexers" because of its selection of signal for transmitting in combination with interfaces 114-117 and logic 119-121*).

Regarding **claim 5**, in addition to features recited in base claim 1 (see rationales discussed above), Drotter further discloses wherein the receiver logic circuit (118-121) comprises a bank of multiplexers (118) each configured to transmit a selected one of all the signals (signal received at 114-117) received in the channels (any of 108-111) (*note: disclosed incoming message buffers is equated to corresponding to "a bank of multiplexers" because of its selection of signal for receiving in combination with interfaces 114-117 and logic 119-121*).

Regarding **claim 6**, in addition to features recited in base claim 1 (see rationales discussed above), Drotter further discloses wherein the symbols are insensitive to signal inversion (*col. 4, line 62 to col. 5, line 2, Drotter discloses when the expected cell on port 114 does not arrive, the receiver advances port 115 to the top of the round-robin order, overriding and resetting sequence number and round-robin expectation. The recitation thereat reads on the claimed limitation*).

Regarding **claim 7**, in addition to features recited in base claim 1 (see rationales discussed above), Drotter further discloses wherein the symbols are 10-bit lane identifiers compatible with an 8B/10B encoding scheme (*note: at col. 3, lines 38-44, Drotter discloses the patented invention is applicable in the Infiniband environment (HCA and TCA). Thus, it is inherent the discussed symbols are corresponding to the claimed limitation for the claimed limitations are encompassed by the Infiniband standard*).

Regarding **claim 8**, in addition to features recited in base claim 1 (see rationales discussed above), Drotter further discloses wherein the channel order correction (cell synchronization) is performed while a first set and a second set of training data (skipped cells) are transmitted through the link (*col. 5, lines 3-20 reading in reference to Fig. 9)*

Regarding **claim 10**, in accordance with Drotter reference entirety, Drotter discloses a method for correcting the order of data signals received via a plurality channels (108-111), wherein the method comprises:

transmitting (100) symbols (cells) across the plurality of channels (108-111), wherein the symbols are unique to each channel (*col. 3, lines 50-54*); and

ordering (119) the channels so that the unique symbols arrive at respective predetermined buffers (118) (*col. 3, lines 55-60*).

Regarding **claim 11**, in addition to features recited in base claim 10 (see rationales discussed above), Drotter further discloses wherein the plurality of channels are part of a communications link (112) comprising a transmitter port (any of 104-07 and 101-103) and a receiver port (any of 114-117 and 118-121) wherein: the receiver port

comprises a lane reorder circuit (119) that is configured to reroute the channel signals if the receiver port detects an unexpected channel symbol in the signals transmitted by the transmitter port (*col. 4, lines 29-55*); and a transmit port comprising a lane reorder circuit (103) that is configured to reroute the channel signals if the transmit port does not detect a predetermined response from the receiver port (*col. 3, line 46 to col. 4, line 11*).

Regarding **claim 14**, in accordance with Drotter reference entirety, Drotter discloses a computer network (Fig. 4) that comprises:

a first device (100) having a first adapter (*101-102 and 104-107*);

a second device (113) having a second adapter (114-117 and 118-121) coupled to (108-111) the first adapter by a communications link (112) having one or more serial lanes (108-111), the second adapter having a multilane transmit path and a multilane receive path, wherein the multilane receive path includes a lane reorder circuit (118-121) configured to reorder the lanes of the multilane receive path if misordering is detected (*col. 3, line 55 to col. 5, line 20*).

Regarding **claim 15**, in addition to features recited in base claim 14 (see rationales discussed above), Drotter further discloses wherein the multilane receive path further includes:

a plurality of receive buffers (118) coupled via the reorder circuit (119-121) to the communications link serial lanes (108-111); and a reconstruction circuit (119-121) configured to retrieve symbols from the plurality of receive buffers (118) to form an output sequence of received symbols (cells), wherein the reconstitution circuit is configured to examine lane identifier symbols (BSNs) in training packets (skipped cells)

received via the communications link to detect misordering of the lanes (*col. 5, lines 3-19*).

Regarding **claim 16**, in addition to features recited in base claim 15 (see rationales discussed above), Drotter wherein when misordering is detected the reorder circuit is configured to adjust the coupling between the serial lanes and the receive buffers to compensate for the misordering (*col. 5, lines 3-35*).

Regarding **claim 17**, in addition to features recited in base claim 14 (see rationales discussed above), Drotter wherein the reorder circuit is configured to couple the communication link serial lanes to the lanes of the multilane receive path (*see Fig. 4 for network connection*).

Regarding **claim 18**, in addition to features recited in base claim 14 (see rationales discussed above), Drotter wherein the first adapter (100) includes a multilane transmit path (103 and 104-107) and a multilane receive path (104-107 and 103), wherein the multilane receive path includes a lane reorder circuit configured to reorder the lanes of the multilane receive path if the second adapter is not receiving or is incorrectly receiving signals transmitted from the first adapter to the second adapter (*col. 5, lines 3-19*).

Allowable Subject Matter

5. Claims 9 and 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record, considered individually or in combination, fails to fairly show or suggest the claimed invention of base claims 1 and 10 and further limit with a training set data comprising COMMA delimiter and LANE identifier symbol in a manner as disclosed in the specification and recited in claims 9 and 12-13.

Conclusion

7. The prior/related art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bunton et al (USP 6,690,757).

Kagan et al (USP 6,243,787).

Ward (USP 6,549,540).

Henson (USP 6,158,014).

Gallagher et al (USP 5,619,497).

Hsu et al (USP 5,304,996).

Infiniband Architecture Specification Volume 2 Release 1.0, Chapter 5: Link/Phy Interface, pages 1-5 and 65-131, October 2000.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frank Duong whose telephone number is (571) 272-3164. The examiner can normally be reached on 7:00AM-3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Frank Duong
Examiner
Art Unit 2666

September 23, 2004